Claims and Abstract for US Filing - -

What is claimed is:

1. A method for forming an in-situ wafer scale polymer stud grid array, the method comprising:

providing a semiconductor wafer with integrated circuit device areas, the integrated circuit device areas having exposed bond pads and wafer passivation, and applying one or more metal film depositions over the bond pads and the wafer passivation;

patterning the one or more metal film depositions extending over the exposed bond pads and the wafer passivation to create metal film segments in desired locations over the bond pads to perform as bond pad cover metallurgy;

coating the semiconductor wafer with a first polymer layer processed to form raised studs having stud tip contacts in desired locations on the surface of each of the integrated circuit device areas;

removing regions of the first polymer layer to expose a central portion of underlying bond pad cover metallurgy;

processing the first polymer layer to clean and prepare the exposed central portion of the underlying bond pad cover metallurgy for adhesion to subsequently applied metal layers;

processing the first polymer layer for high conductor adhesion;

applying a metal coating to the semiconductor wafer to cover at least all exposed pad cover metallurgy areas and all exposed regions of the first polymer layer;

thickening the metal coating and forming an interconnect circuit thereon;

forming a second polymer layer over selected areas of the metal coating; and

depositing a barrier layer and an oxidation protection layer on exposed areas of the metal coating.

2. The method of claim 1, wherein the step of coating the semiconductor wafer with a first polymer layer comprises forming the first polymer layer to be thinner in regions between the integrated circuit device areas.

3. The method of claim 1, wherein the first polymer layer is removed in selected regions over the bond pad cover metallurgy and in regions between the integrated circuit device areas, by one of laser ablation, photolithography, reactive ion etching, or plasma etching.

4. The method of claim 1, further comprising roughening the bond pad cover metallurgy by one of chemical microetching or plasma microetching.

5. The method of claim 1, wherein coating the surface of the wafer with metal comprises one of sputtering, chemical vapor deposition, electroless plating, or a combination thereof.

6. The method of claim 1, wherein the step of thickening the metal coating comprises processing by electrolytic plating.

7. The method of claim 1, wherein the step of applying the second polymer layer excludes covering the stud tip contacts, saw path streets between the integrated circuit device areas and desired bond pads.

8. The method of claim 1, wherein the step of forming the second polymer layer comprises one of spin coating, spraying, dispensing or film lamination.

9. The method of claim 8, further comprising removing the second polymer layer from desired locations, by one of dry processing or wet processing.

10. The method of claim 1, wherein the step of metal plating comprises sputtering through a metal mask.

11. The method of claim 1, wherein the metal comprises copper.

12. The method of claim 1, wherein the pad cover metallurgy is formed by depositing electroless Ni to cover only the bond pads and the perimeter passivation area, and depositing a Au layer onto the Ni surface.

13. A method for forming an in-situ wafer scale polymer stud grid array on a semiconductor wafer having integrated circuit device areas, the integrated circuit device areas having patterned pad cover metallurgy regions, exposed bond pads and wafer passivation, the method comprising:

applying one or more metal film depositions over the exposed bond pads and the wafer passivation;

processing the one or more metal film depositions extending over the exposed bond pads and the wafer passivation across the semiconductor wafer to create metal film segments in desired locations over the exposed bond pads to perform as bond pad cover metallurgy;

placing the semiconductor wafer in a tooling plate which provides an annular ring region about the wafer, wherein one surface of the annular ring region is substantially coplanar with the surface of the wafer;

coating the semiconductor wafer and a desired portion of the surface of the tooling plate annular ring region with a first polymer layer processed to form raised studs at desired locations across the surface of each of the integrated circuit device areas;

removing regions of the first polymer layer to expose a central portion of underlying bond pad cover metallurgy;

processing the semiconductor wafer to clean and prepare the exposed central portion of the underlying bond pad cover metallurgy for adhesion to subsequently applied metal layers;

processing the first polymer layer for high conductor adhesion;

applying a metal coating over the semiconductor wafer and the annular ring region of the surrounding tooling plate surface covering at least all exposed pad cover metallurgy areas and all exposed regions of the first polymer layer;

coating the active surface of the semiconductor wafer with one or more metal films;

thickening the metal coating and forming an interconnect circuit thereon;

forming a second polymer layer over selected areas of the metal coating and selected regions of the exposed first polymer layer; and

depositing a barrier layer and an oxidation protection layer on exposed areas of the metal coating, and forming a circuit pattern about the semiconductor wafer that is contiguous with desired circuit elements in the metal coating across the active wafer surface and the annular ring region of the tooling plate.

14. The method of claim 13, wherein the step of coating the semiconductor wafer with a first polymer layer comprises forming the polymer coating to be thinner in regions between the integrated circuit device areas.

15. The method of claim 13, wherein the first polymer layer is removed in selected regions over the bond pad cover metallurgy and in regions between the integrated circuit device areas by one of laser ablation, photolitho-

graphy, reactive ion etching, or plasma etching.

16. The method of claim 13, further comprising roughening the second phase metal deposition by one of chemical microetching or plasma microetching.

17. The method of claim 13, wherein the step of coating the surface of the semiconductor wafer with metal comprises one of sputtering, chemical vapor deposition or electroless plating, or a combination thereof.

18. The method of claim 13, wherein the step of thickening the metal coating comprises processing by electrolytic plating.

19. The method of claim 13, wherein the step of applying the second polymer layer excludes covering the stud tip contacts and the saw path streets between the integrated circuit device areas.

20. The method of claim 13, wherein the step of forming the second polymer layer comprises one of spin coating, spraying, dispensing or film lamination.

21. The method of claim 20, further comprising removing the _____ polymer layer from the desired locations, by one of dry processing or wet processing.

22. The method of claim 13, wherein the step of metal plating comprises sputtering through a metal mask.

23. The method of claim 13, wherein the metal comprises copper.

24. The method of claim 13, wherein the pad cover metallurgy is formed by depositing electroless Ni to cover only the bond pads and the perimeter passivation area, and depositing a Au layer onto the Ni surface.

25. An in-situ wafer scale polymer stud grid array structure formed directly on a semiconductor wafer having individual integrated circuit device areas and connecting bond pads thereon, the polymer stud grid array structure comprising:

raised studs in desired locations formed across the surface of each of the integrated circuit device areas;

exposed bond pad cover metallurgy central portions;

one or more metal film depositions covering connecting the bond pads and the raised studs;

a metal layer covering the semiconductor wafer processed to connect desired pad cover metallurgy central portions with studs to form a desired interconnection circuit; and

a polymer layer covering the desired regions of the entire circuit area, such that a barrier layer and an oxidation protection layer of metal covers the exposed metal features, the grid array extending across the entire semiconductor wafer, and metallized studs being disposed across each of the integrated circuit device areas.

26. The structure of claim 25, where in the metal layer comprises copper.

27. An in-situ wafer scale polymer stud grid array structure comprising:

a semiconductor wafer having individual integrated circuit device areas and patterned pad cover metallurgy regions, and coated with a first polymer layer processed to form raised studs in desired locations across the surface of each of the integrated circuit device areas;

exposed bond pad cover metallurgy central portions;

a metal layer covering the semiconductor wafer process to connect desired pad cover metallurgy central portions with studs to form a desired interconnection circuit; and

a second polymer layer covering the entire interconnection circuit area, such that a barrier layer and an oxidation protection layer of metal covers the exposed metal features, the grid array field extends across the entire semiconductor wafer, and the metallized studs are disposed across each of the integrated circuit device areas, the circuit pattern in the film material coating the surface of the annular ring region about the semiconductor wafer is contiguous with desired circuit elements in the material coating the surface of the semiconductor wafer, and the interconnection circuit area extends beyond the edge of the semiconductor wafer.

28. The structure of claim 27, where in the metal layer comprises copper.